IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: DANIEL, Mordechai et al.

Serial No. : 09/782,090

Filed : February 12, 2001

For : METHOD AND APPARATUS FOR EFFICIENT MESSAGING BETWEEN MEMORIES ACROSS A PCI BUS

Group Art Unit 2182
Examiner: NGUYEN, Tanh Q.

Tel Aviv, Israel
July 22, 2004

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 2031

Sir:

DECLARATION UNDER 37 CFR SEC 1.132

I, the undersigned, Michael Ben-Nun, of 20 HaHagana Street, Ramat Hasharon, Israel 47203, hereby declare as follows:

Background Information

1. I am currently an employee of P-Cube Ltd., the assignee of the abovementioned patent application.
I hold the position of the Chief Technology Officer and General Manager of the Israel-based research and development facility.

2. I have previously been employed by the following of USA firms (partial list):

a) Rockwell Semiconductors - General Manager of the Israel design center
b) Digital Equipment Corporation - Technical director and strategic marketing manager
c) National Semiconductor - VLSI design and management

3. My educational qualifications are summarized as:
a) B.Sc. in Electrical Engineering, Tel Aviv University
b) Networking College graduate from Carnegie Mellon, Pittsburgh, USA
c) Executive Education - Insead, Fontainbleau, France
d) Three dozen management, marketing and technology courses/seminars.

4. I am a co-inventor of sixteen (16) issued USA patents, thirteen (13) of which deal with queues and queue management. A list of the patents is hereby attached to the end of this affidavit.

Overview Statements

5. The explanation contained in the following paragraphs addresses the uniqueness of the present invention over prior art solutions. The explanation does not replace the detailed background and operation details that were already provided in the patent application. These explanations are brought here to challenge the relevance of the Examiner's rejection statements.

6. The subject patent application deals with performance improvements achieved by an apparatus and method thereof for the communication over a PCI bus, overcoming its limitation of significantly slower reads in comparison with write operations, across the PCI bus.

7. The object of the invention is achieved by a structure that includes, on the receiver side, a queue with a register defining the length of the queue, a read head pointing to the next to be read data item, and a total read register providing data on the total number of bytes actually read from the circular queue.

In addition, on the transmitter side, there is a register that contains the duplicate information of the circular queue's length, a write head register pointing to the point in the queue into which data is to be written to next, a register containing the information of the total number of bytes actually written into the circular queue, and a total read register which contains a copy of the content of the total read register of the receiver.

8. The object of the invention is further achieved by employing a method whereupon the need of a first unit to read data from a second unit across a bus having characteristics such as the PCI bus, is performed by the use of several write operations. For example, two write operations are performed in accordance with the disclosed invention, to achieve the equivalent read result.

As no read operations are allowed between a first CPU and a second CPU connected by a PCI-like bus, write operations are employed to send messages across the PCI-like bus. For example, a first CPU may write to a second CPU a message requesting to read data from that second CPU (a first write operation) and thereafter the second CPU sends a message to the first CPU with the required content (a second write operation). Each write operation is performed as disclosed in the patent application.

9. Furthermore, the first CPU and the second CPU communicate with each other through a series of messages, and further through controls "LP" and "FM". Each of "LP" and "FM" further contain a magic number that enables the verification of the queue management.

10. The concept of "magic numbers" is well-known in the art, and I hereby declare that I am aware of such techniques. The Examiner may wish to refer to US patent 6,668, 291 by Forin et al., and assigned to Microsoft Corporation, to learn that the existence of the term "magic number" is sufficiently well-known in the art so as not to require any further explanation other than use of the term. The Examiner may further wish to review US patent 6,606,628 by Monesen et al., and assigned to Cisco Technology, Inc., where it is noted that "*...a "magic number" means any identifying number that can indicate whether a given block is a valid file system block.*" (column 3, lines 1-3).

11. An example of the application of the "magic number" for queue management is given in the specification at p. 13, line 29, where it is stated "the magic number is checked 630 for validity." This matches paragraph 10 above.

Reply to the Examiner's Rejection Statements- Specification

12. For purposes of this affidavit, a portion of the specification is reproduced below with numbered sentences:

Page 9, beginning at line 6:
(1) *"The last message of the last data is followed by a stopper designator separator, which is marked as "FM", wherein F represents a hexadecimal numerical value and M represents a predefined magic number."*

Page 9, beginning at line 9:
(2) *"The 'LP' contains at least a length field, designating the amount of data to be read in the following message. Usually this is a number of bytes to be read. It further contains a predefined identification number, also known as a 'magic number', which is used by the system to verify correctness of the queue management."*

Page 9, beginning at line 19:
(3) *The "FM" is comprised at least of a stopper designator, which is a predefined numerical value, followed by the predefined magic number."*

13. The Examiner incorrectly objects to the amendment filed on April 1, 2004 claiming it introduces new matter into the disclosure. The Examiner notes that:

"The original disclosure only supports a magic number in both a header-type separator and a stopper-type separator,"

and then the Examiner erroneously concludes

"...which indicates to the examiner that the magic number in the header-type separator is the same magic number that is in the stopper type separator".

I have reviewed the application prior to the filing of the amendments and found that in sentence (1) reproduced above, there is mentioned "*a predefined magic number*."

In sentence (2) above, there is mentioned "*a predefined identification number, also known as a 'magic number'...*"

As a person skilled in the art my conclusion is that the magic numbers described by the specification of the application are two separate magic numbers, and I have underlined in the text above the words that lead to my conclusion.

This would not preclude, in a particular case, having both magic numbers of the "LP" and the "FM" be identical. Seemingly, the Examiner has confused the requirement of having a magic number in both "LP" and "FM", which is correct, with a requirement that both of these are identical, which is false.

Reply to the Examiner's Rejection Statements - Claim Rejection Under 35 USC 112

14. The Examiner incorrectly rejects claims 18-19 under the first paragraph of 35 USC 112 for failing to comply with the written description requirement. Being a person skilled in the art, I hereby declare that to the best of my judgement, the subject matter of both claims 18 and 19 was disclosed in the application as filed and as further shown below.

15. As for claim 18, Examiner asserts that it is not shown that the inventors, at the time the application was filed, had possession of the claimed invention of the stopper separator containing a stopper magic number. The Examiner further refers to his objection to the amendments in the specification. Claim 18, as amended states:

"The system of claim 17 where said stopper separator further contains a predefined stopper "magic" number."

In the application as filed, prior to the proposed amendments I found that sentences (1) and (3) reproduced above, describe:

"...a *stopper designator separator, which is marked as "FM,"* and

"*The "FM" is comprised at least of a stopper designator, which is a predefined numerical value, followed by the predefined magic number.*"

As a person skilled in the art, I understand that the original specification contains the subject matter claimed in claim 18, and this can be further noted from the underlined sections. It is clear to me that the use of the words "*the predefined magic number*" in sentence (3) refers to the magic number of the "FM" and not the magic number of the "LP".

I further acknowledge that the amendments to the specification did not introduce any new subject matter not previously contained in the specification as filed.

16. As for claim 19, the same logic applied for claim 18 in item #13 above applies equally to this claim.

17. The Examiner incorrectly rejects claims 1, 4, and 10-19 under the first paragraph of 35 USC 112 claiming that the write operations performed by the transmitting CPU, as claimed, do not enable the receiving CPU to achieve a read operation.

Being a person skilled in the art, I hereby declare that I understand that the specification supports the claims and enables a person skilled in the art to achieve a read operation using only write operations.

As an example, assuming that CPU A is to read data from CPU B over a bus. A read operation is a well-known prior art solution, however, in the case of PCI-type busses, this is a time consuming operation.

In accordance with the invention, instead of performing a read operation, CPU A (transmitting CPU 210) would first perform a first write operation in the manner disclosed in the invention, specifically, sending a first message, to CPU B (receiving CPU 200). The first message would contain a request to provide the desired data portion. The exact content of the first message is not part of the invention but a person skilled in the art would be able to easily implement a message system to perform such a task.

As a result of receiving the message, a second write operation occurs in the manner disclosed in the invention, specifically, a second message is sent, to CPU A. The second message would contain the desired data to be read by CPU A. The exact content of the second message is not part of the invention but a person skilled in the art would be able to easily implement a message system to perform such a task.

In the specification, at page 6, line 4, it is stated:

"*In the exemplary embodiments described hereinbelow and with reference to the Figures, there is shown an apparatus*

and method which accomplishes the transmission of a data message from a transmitting CPU to a receiving CPU across a data bus, using a series of write operations and with no read operations being performed across the said data bus."

This statement in the specification clearly indicates that there is a need to use multiple write operations to achieve the result of a read operation.

Reply to the Examiner's Rejection Statements - Response to Arguments

18. The Examiner incorrectly cites Daniel et. al (USP 6,115,761) against the disclosed invention.

Daniel discloses a relatively complex credits system for managing the operation of a FIFO memory. This is used for the purpose of transferring data between two units. Because a FIFO access routine across a bus may cause a significant system performance bottleneck, in addition there is a use of a pointer per processor for a dual descriptor FIFO arrangement.

According to Daniel et al, using the credits system it is possible to determine if the FIFO of the other side is available without accessing the bus.

By contrast, the disclosed invention makes use of a "total read" and "total write" registers, resulting in what I would conclude to be an entirely different queue management solution clearly differentiated from that which is disclosed by Daniel.

19. The Examiner also incorrectly cites Daniel in view of Young against the claims of the invention.

Young clearly describes a system that is different from the disclosed invention by at least its architecture.

Specifically, I conclude that Young's "queued TCB counter 117" and Young's "queued TCB counter 131", are two "total write" registers as termed in the invention.

I further conclude that Young discloses a single "removed TCB counter 132", which is one "total read" register in the terms of the disclosed invention.

By contrast, in the invention we can easily find (see Fig. 2) that the invention discloses a single "total write" register and two "total read" registers.

Furthermore, I conclude that the system disclosed by Young requires at least one read operation for the purpose of reading the content of circular queue 112. This is a result of the choice of use of registers made by Young causing the system to perform a read across a PCI bus that, in accordance with the present invention, must be avoided.

20. This declaration is given in support of the patent prosecution efforts made in prosecution before the USPTO.

21. I declare that all the statements made herein of my own knowledge are true, and that all statements made on information and knowledge are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Sec. 1001 of Title 18 of the United States Code, and the willful false statements may jeopardize the validity of the application and any patent issuing threon.

Signed this 22 day of July 2004.

Michael Ben-Nun